

What is claimed is:

1 1. A method for charge control of a photoflash
2 capacitor comprising the steps of:

3 detecting a voltage on the photoflash capacitor;
4 asserting and then latching a recharge signal when the
5 detected voltage is lower than a first reference
6 voltage;

7 de-asserting and then latching the recharge signal when
8 the detected voltage is higher than a second
9 reference voltage;

10 charging the photoflash capacitor when the recharge
11 signal is asserted; and

12 providing a pin for connection of a resistive element
13 which determines the first reference voltage.

1 2. The method as claimed in claim 1 further
2 comprising the steps of:

3 asserting and de-asserting a first output signal
4 respectively when the detected voltage is lower
5 and higher than the first reference voltage;

6 asserting and de-asserting a second output signal
7 respectively when the detected voltage is higher
8 and lower than the second reference voltage;

9 asserting the recharge signal when the first output
10 signal is asserted, until the second output
11 signal is asserted; and

12 de-asserting the recharge signal when the first output
13 signal is asserted, until the first output signal
14 is asserted.

1 3. A photoflash capacitor charger operating in
2 conjunction with a microprocessor, comprising:

3 a transformer receiving a primary input voltage to
4 induce a secondary output voltage on a photoflash
5 capacitor when a recharge signal is asserted; and
6 a recharge controller detecting a voltage on the
7 photoflash capacitor, asserting and then latching
8 the recharge signal when the detected voltage is
9 lower than a first reference voltage, and de-
10 asserting and then latching the recharge signal
11 when the detected voltage is higher than a second
12 reference voltage;

13 wherein the first reference voltage is determined by
14 the microprocessor.

1 4. The photoflash capacitor charger as claimed in
2 claim 3, wherein the recharge controller comprises:

3 a first comparator circuit asserting and de-asserting a
4 first output signal respectively when the
5 detected voltage is lower and higher than the
6 first reference voltage;

7 a second comparator circuit asserting and de-asserting
8 a second output signal respectively when the
9 detected voltage is higher and lower than the
10 second reference voltage; and

11 a latch asserting the recharge signal when the first
12 output signal is asserted, until the second
13 output signal is asserted, and de-asserting the
14 recharge signal when the second output signal is

15 asserted, until the first output signal is
16 asserted.

1 5. The photoflash capacitor charger as claimed in
2 claim 4, wherein the first comparator circuit comprises:
3 a voltage divider having a first and second resistor
4 connected in series, and receiving the primary
5 input voltage and generating the first reference
6 voltage divided therefrom; and
7 a comparator having a positive input receiving the
8 first reference voltage and a negative input
9 receiving the detected voltage, and outputting
10 the first output signal;
11 wherein one of the first and second resistor is
12 adjustable.

1 6. The photoflash capacitor charger as claimed in
2 claim 4, wherein the second comparator circuit comprises:
3 a voltage divider having a first and second resistor
4 connected in series, and receiving the primary
5 input voltage and generating the second reference
6 voltage divided therefrom; and
7 a comparator having a positive input receiving the
8 detected voltage and a negative input receiving
9 the second reference voltage, and outputting the
10 second output signal.

1 7. The photoflash capacitor charger as claimed in
2 claim 4, wherein the latch comprises:

3 a first and second inverter wherein an input and output
4 of the first inverter are respectively coupled to
5 an output and input of the second inverter;
6 a third inverter having an input coupled to the output
7 of the second inverter and outputting the
8 recharge signal;
9 a first switch coupled between the input of the first
10 inverter and the ground, and closed and opened
11 respectively when the first recharge signal is
12 asserted and de-asserted; and
13 a second switch coupled between the input of the second
14 inverter and the ground, and closed and opened
15 respectively when the second output signal is
16 asserted and de-asserted.

1 8. The photoflash capacitor charger as claimed in
2 claim 7, wherein each of the first, second and third
3 inverter comprises:

4 a transistor having a collector as the output and an
5 emitter coupled to the ground;
6 a current source coupled to the collector of the
7 transistor; and
8 a resistor having one end as the input and the other
9 end coupled to a base of the transistor.

1 9. The photoflash capacitor charger as claimed in
2 claim 7, wherein each of the first and second switch is a
3 transistor.

1 10. The photoflash capacitor charger as claimed in
2 claim 3 further comprising a voltage divider coupled with

3 the photoflash capacitor in parallel, having a first and
4 second resistor connected in series, and generating the
5 detected voltage divided from a voltage difference across
6 the photoflash capacitor.

1 11. An integrated circuit for recharge control of a
2 photoflash capacitor, comprising:

3 first, second, third and fourth pins respectively for
4 reception of a ground voltage, primary input
5 voltage, detected voltage from the photoflash
6 capacitor and connection with a resistive
7 element;

8 a first comparator circuit comprising:

9 a first comparator having a positive and negative
10 input respectively connected to the fourth
11 and third pin; and

12 a resistor connected between the second and fourth
13 pin;

14 a second comparator circuit comprising:

15 a voltage divider connected between the first and
16 second pins; and

17 a second comparator having a positive and negative
18 input respectively connected to the third
19 pin and an output of the voltage divider;
20 and

21 a latch comprising:

22 a first and second inverter wherein an input and
23 output of the first inverter are
24 respectively connected to an output and
25 input of the second inverter;

26 a third inverter having an input connected to the
27 output of the second inverter and an output
28 for a recharge signal;
29 a first switch connected between the input of the
30 first inverter and the first pin; and
31 a second switch connected between the input of the
32 second inverter and the first pin.

1 12. The integrated circuit as claimed in claim 11,
2 wherein each of the first, second and third inverters
3 comprises:

4 a transistor having a collector as the output and an
5 emitter connected to the first pin;
6 a current source connected to the collector of the
7 transistor; and
8 a resistor having one end as the input and the other
9 end connected to a base of the transistor.

1 13. The integrated circuit as claimed in claim 11,
2 wherein each of the first and second switch is a transistor.

1 14. The integrated circuit as claimed in claim 11
2 further comprising:

3 a fifth pin for connection with a primary winding of a
4 transformer; and
5 a current switch controlled by the recharge signal from
6 the third inverter and connected between the
7 fifth and first pins.